Customer No.: 31561
Application No.: 10/707,677
Docket NO.: 12089-US-PA

AMENDMENTS

In the Claims:

Claims 1-6. **Cancelled.**

Claim 7. (Currently amended) A multi-level memory cell, comprising:

a substrate;

a gate disposed over the substrate;

a source region and a drain region configured in the substrate on each side of the gate;

a tunneling dielectric layer disposed between the gate and the substrate;

a charge-trapping layer disposed between the tunneling dielectric layer and the gate; and

a top dielectric layer disposed between the charge-trapping layer and the gate, wherein the top dielectric layer has at least two portions from the source region to the drain region, and the portions adjacent to the source region has~~ve~~ a different thicknesses to that of the portion adjacent to the drain region, and wherein the tunneling dielectric layer has substantially a same thickness from the source region to the drain region.

Claim 8. (previously presented) The multi-level memory cell of claim 7, wherein a material constituting the charge-trapping layer comprises silicon nitride.

Claim 9. (original) The multi-level memory cell of claim 7, wherein the cell

further comprises a pair of spacers disposed on each sidewall of the gate.

Claim 10. (previously presented) The multi-level memory cell of claim 9, wherein the cell further comprises lightly doped regions configured in the substrate underneath the spacers.

Claim 11. (previously presented) The multi-level memory cell of claim 9, wherein a material constituting the spacers comprises silicon oxide.

Claim 12. (original) The multi-level memory cell of claim 7, wherein the tunneling dielectric layer has a thickness between about 20Å to 40Å.

Claim 13. (original) The multi-level memory cell of claim 7, wherein the charge-trapping layer has a thickness between about 40Å to 60Å.

Claim 14. (previously presented) The multi-level memory cell of claim 7, wherein a material constituting the tunneling dielectric layer comprises silicon oxide.

Claim 15. (previously presented) The multi-level memory cell of claim 7, wherein a material constituting the top dielectric layer comprises silicon oxide.